Session 8 Overview

DRAM and TCAM

Chair: Terry Lee, Micron Technology, Boise, ID

Associate Chair: Young-Hyun Jun, Samsung, Hwasung-City, Korea

The global demand for bandwidth- and media-rich content has increased in unison with higher penetration rates of broadband Internet. The triple play of voice, data, and video content puts greater demands on CPU performance, graphics processing power, and networking router efficiency. In addition, the consumer appetite for mobile appliances dictates new requirements for power-efficient architectures. These application trends are driving more stringent requirements for memory subsystem performance, and future memory devices must deliver higher data rates, lower latencies, and greater power efficiency. The presentations in this session will report recent advances in DRAM and TCAM technologies that address these challenges.

In Paper 8.1, a deca-data rate DRAM is introduced that effectively hides the CRC overhead thereby enabling secure transmission of 8Gb/s/pin data over a differential I/O interface. This DRAM data rate is 25% higher than previously reported.

Graphic rendering times are very sensitive to memory bandwidth, and the GDDR3 SDRAM delivers this bandwidth with high data rate, single-ended wide I/O devices. The next two papers of the session, Papers 8.2 and 8.3, solve these technical challenges. A 2.0Gb/s/pin 512Mb device has been implemented in a 0.11μm process that improves output jitter by reducing the simultaneous switching outputs (SSO) to one-third through pad-driver averaging. Additional jitter improvements are gained by damping power-supply oscillations. A 2.5Gb/s/pin 256Mb GDDR3 device in a 0.10μm process is also described that implements an improved series pipelined CAS latency control and dual-loop DLL with low-power duty-cycle-correction circuitry.

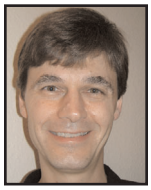
The next paper of the session, Paper 8.4, provides insight into the next-generation of main memory technology, DDR3. Dual-core CPUs have been developed to keep up with the higher processing demands, but they require greater memory subsystem bandwidth and lower latencies to realize system performance improvements. Details of a 512Mb DDR3 device that double the data rates over DDR2 and reduce address access time from 11.3ns to 8.4ns, are explored.

Mobile electronics require lower standby-current DRAMs to extend battery life. In Paper 8.5, a low-power embedded DRAM is discussed that includes an extended data-retention sleep mode to improve retention times by 8× and reduce the leakage current to 13% of normal operation. The performance improvement is achieved with a 65nm multi-threshold CMOS process and memory array ECC scrubbing.

High aggregate network traffic requires high-speed IP lookup tables that minimize power during search operations. In Paper 8.6, a new TCAM architecture leverages the use of don't-care bits in the table to implement an improved segmented search-line topology. A 1.1ns search-time with 0.35fJ/bit search energy is estimated. A second TCAM device, in Paper 8.7, uses a range-matching cell with compare operations and a search-line charge-recycling technique to improve storage efficiency by 2.5× compared to conventional TCAMs while reducing the search-line power to 40% of a precharged TCAM.

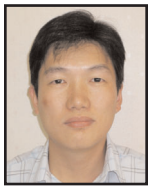
8.1 An 8Gb/s/pin 9.6ns Row-Cycle 288Mb Deca-Data Rate SDRAM with an I/O Error-Detection Scheme **8:30 AM**
K-H. Kim, Samsung, Hwasung-City, Geyonggi-Do, Korea

A 288Mb deca-data rate SDRAM with an I/O error-detection scheme is developed. Deca-data rate is proposed to include CRC for the higher data-rate beyond 5Gb/s/pin using a conventional DRAM process. Several techniques, including an area-efficient cell array consisting of two $6F^2$ cells are adopted to enhance the core cycle speed. Measurement results show that the chip has a peak read or write bandwidth of 6.4GB/s and row-cycle time (t_{RC}) of 9.6ns with a 1.6V supply.



8.2 A 2Gb/s/pin 512Mb Graphics DRAM with Noise-Reduction Techniques **9:00 AM**
M. Brox, Infineon, Munich, Germany

A 512Mb DRAM operates up to a data-rate of 2Gb/s/pin. It employs an averaging pad-driver design which reduces simultaneous switching noise to one third of a conventional design. Resistive damping elements eliminate the level degradation of the receivers caused by an oscillation of the on-chip ground. A technique for cancelling line-to-line coupling noise is also described.



8.3 A 2.5Gb/s/pin 256Mb GDDR3 SDRAM with Series Pipelined CAS Latency Control and Dual-Loop Digital DLL **9:30 AM**
D. Lee, Hynix Semiconductor, Ichon, Korea

A series pipelined CAS latency control with voltage-controlled delay line that extends maximum data rate to 2.5Gb/s/pin at 1.7V, is presented. Other schemes applied in the DLL are dual loop control that increases power noise immunity and LPDCC that achieves low power consumption. All these schemes are implemented in a 8Mx32 device using a 0.10µm DRAM process.

8.4 An 8.4ns Column-Access 1.3Gb/s/pin DDR3 SDRAM with an 8:4 Multiplexed Data-Transfer Scheme **10:00 AM**
H. Fujisawa, Elpida Memory, Sagamihara, Japan

The column access time of a 512Mb DDR3 SDRAM implemented in a 90nm dual-gate CMOS process is reduced by 2.9ns to 8.4ns through an 8:4 multiplexed data-transfer scheme that enables the use of shielded I/O lines. A dual-clock additive latency counter enables a 30% reduction in cycle time from 1.7 to 1.2ns. By combining these with a multiple on-die-termination merged output driver, 1.3Gb/s/pin operation at 1.36V and a column latency of 6 (CL6) is achieved.

8.5 A 65nm Low-Power Embedded DRAM with Extended Data-Retention Sleep Mode **10:45 AM**
T. Nagai, Toshiba, Kawasaki, Japan

An extended data retention (EDR) sleep mode with ECC and MT-CMOS is proposed for embedded DRAM power reduction. In sleep mode, the retention time improves by 8 times and the leakage current is reduced to 13% of the normal operation mode. Since ECC scrubbing operates only in the EDR sleep mode, read/write performance is not degraded. A 65nm low-power embedded DRAM macro featuring 400MHz operation and 0.39mW of data-retention power is realized.

8.6 TCAM for IP-Address Lookup Using Tree-Style AND-type Match Lines and Segmented Search Lines **11:15 AM**
C-C. Wang, National Chung Cheng University, ChiaYi, Taiwan

Tree-style AND-type match-line and segmented search-line schemes cooperatively improve TCAM speed and energy efficiency for applications like IP-address lookup in a network router. Fabricated in a 0.13µm process, the TCAM achieves 1.10ns search time with 0.348fJ/b/search.

8.7 A Storage- and Power-Efficient Range-Matching TCAM for Packet Classification **11:45 AM**
Y-D. Kim, Seoul National University, Seoul, Korea

A range-matching TCAM using the proposed range-matching cell increases storage efficiency by up to 2.5 times compared to a conventional TCAM. In addition, charge recycling with the proposed static TCAM cell can reduce the search-line power. The 512×144b prototype chip, fabricated in a 1.2V 0.13µm CMOS process, achieves a 4.8ns search time at 0.59fJ/b/search.